REMARKS

In response to the Office Action mailed August 27, 2003, Applicant respectfully requests reconsideration. To further the prosecution of this application, Applicant submits amendments and arguments herewith.

Claims 1-6 were pending in this application. By this amendment, Applicant has amended claims 1-4, 8, and 9 for the sole purpose of clarification. Claims 13-16 have been cancelled without prejudice or disclaimer. Accordingly, claims 1-12 are pending for examination, with claim 1 being an independent claim.

I. Objections to the Drawings

The drawings are objected to under 37 CFR 1.83(a) for purportedly failing to show every feature of the invention specified in the claims. Applicant respectfully disagrees.

Embodiments of the invention are directed to components in a substrate that associate diffused-type MOS power transistors and logic circuits (page 1, lines 14-17). Figure 1 illustrates a conventional structure of a component that associates a vertical MOS transistor and logic circuits (page 4, lines 17-18). The structure has a drain metallization D that is generally biased to a positive potential with respect a source terminal S (page 1, lines 28-33). In the example of Figure 1, source terminal S is connected to ground via a load L (page 2, lines 18-19). Elements of logic circuits are formed in wells, for example transistor 11 formed in well 10 (page 2, lines 1-3). A ground connection may be implemented to allow proper operation of the components formed in the logic well (page 2, lines 4-7). As an example, ground connection 21 is connected to contact 12 (page 2, lines 17-18). If the drain metallization is negatively biased with respect to the source terminal S, instead of the general positive biasing, a destructive current is likely to flow through the diode formed by the junction of substrate 1 and well 10 (page 2, lines 15-16; lines 27-30).

Figure 2 shows an example of an assembly of the component shown in Figure 1. Battery 23 may be connected to the drain terminal D (page 2, lines 19-21). Diode D2 corresponds to the junction between substrate 1 and well 10 (page 2, lines 15-16). Diode D1 corresponds to the junction between substrate 1 and region 5 (page 2, lines 12-14). The source terminal S of

transistor T is connected to ground via the load L. The logic components in well 10 are not shown. As discussed above, if the polarity of battery 23 becomes reversed, diode D2 will become forward biased, and a destructive current may flow through well 10, indicated in Figure 2 by arrow 24 (page 2, lines 27-30). If the battery 23 is positively biased, but becomes disconnected, a current will flow through the circuit due to the inductive load L, as indicated by arrow 26 (page 3, lines 1-4).

Embodiments of the present invention provide a structure for ground connection of the logic well which does not adversely affect the normal state operation, which prevents the current flow in the logic circuit in case of a battery inversion, and which lets through the current resulting from a battery disconnection (page 3, lines 27-31). Figure 3 shows an example of a logic well ground connection structure according to the present invention. Figures 4A and 4B show equivalent diagrams associated with the ground connection structure according to the present invention.

Claim 1 is directed to a circuit comprising an input to receive a supply voltage, the supply voltage having a normal polarity and an inverted polarity, an output to drive a load, the load being connected between the output and a ground, a logic component, connected between the input and the output, to electrically couple the load to the supply voltage when the supply voltage has the normal polarity, and a first component, connected between the input and the ground, to prevent a first current from flowing in the circuit when the supply voltage has the inverted polarity, and to allow a second non-destructive current to flow in the circuit if the supply voltage is disconnected from the input. As now discussed, each limitation of the claims is shown in the figures.

Referring to Figure 2, the input to receive a supply voltage is illustrated, for example, as terminal D. The output to drive a load is illustrated, for example, as terminal S. The load is illustrated, for example, as L. The claimed logic component, for example, is shown as transistor T. The claimed first component is illustrated, for example, as the ground structure in Figure 3, or in circuit form in Figures 4A and 4B. The direction of the first and second currents is shown, for example, by arrows 21 and 26, respectively, in Figure 2. Thus, all claim limitations are clearly

shown in the figures, and Applicant respectfully requests that the objection to the drawings be withdrawn.

II. Claim Rejections

Claims 1-16 stand rejected under 35 U.S.C. §112, first and second paragraphs, as purportedly failing to comply with the written description requirement and for purportedly being indefinite. Applicant respectfully traverses these rejection.

Page 3 of the Office Action asserts that it is not clear what the first and second currents are. Applicant respectfully disagrees. As discussed above, the direction of the first current is shown in Figure 2, for example, as arrow 21, and corresponds to the current that flows through diode D2 when the diode is forward biased. The direction of the second current is shown, for example, as arrow 26 in Figure 2.

With regard to the rejection raised on page 3, paragraph 2 of the Office Action, Applicant respectfully asserts that the claimed subject matter is not indefinite. Accordingly, Applicant respectfully requests that the rejections of claims 1-12 under 35 U.S.C. §112, first and second paragraphs, be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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